# METHOD OF SUPPRESSING THE EFFECT OF SHINING SPOTS PRESENT AT THE EDGE OF A WAFER

## BACKGROUND OF THE INVENTION

**[0001]** The present invention is directed to semiconductor devices and, more particularly, to methods of fabricating semiconductor devices.

**[0002]** As semiconductor devices have become increasingly smaller, prevention of the contamination of the processing tools and exposure tools used to fabricate the devices has become more critical to avoid the introduction of defects on the semiconductor devices which reduce process yields. As an example, dynamic random access memory (DRAM) devices are prone to reduced yields caused by particulate contamination generated by "shining spots" formed at the periphery of the wafer.

**[0003]** The shining spots are exposed silicon regions formed at the edge of the wafers. DRAM devices typically include a semiconductor memory cell array formed of a plurality of memory cells arranged in rows and columns which are connected by a plurality of bit lines as well as a plurality of word lines. For vertical device memory cells, each cell is comprised of a deep trench region wherein a trench capacitor and a vertical transistor are formed. Each deep trench also divides an active area region. The bit lines contact the active area regions on each side of a deep trench at locations where the active area regions form the drains of the vertical transistors. The word lines pass between the active area regions at locations above the deep trench regions, namely where the active area regions are interrupted, to contact the gates of the vertical transistors formed within the deep trenches.

**[0004]** To form the deep trenches, a pad oxide layer and a pad nitride layer are successively deposited atop a substrate, and then a hard mask layer is deposited atop the nitride layer. A layer of photoresist or other resist is deposited atop the hard mask layer and is then exposed and developed in

a known manner and used to mask the patterning of the hard mask layer as well as the pad nitride layer and the pad oxide layer. Next, the hard mask layer is used to mask the etching of the deep trench, and the hard mask layer is then removed.

**[0005]** While the deep trench is etched, the shining spots are often formed at the periphery of the wafer, typically about 3-4 mm from the edge of the wafer. The shining spots result from a center-to-edge loading effect during the reactive ion etch (RIE) of the deep trench which causes a higher etch rate of the hard mask layer in the regions nearer to the edge of the right wafer than at the center of the wafer. As a result, some or all of the hard mask layer is removed in the regions near the edge of the wafer and exposes the underlying silicon in these regions during at least part of the deep trench etch. The exposed silicon regions near the edge of the wafer are known as "shining spots". The exposed silicon is prone to being broken off and cause particulate contamination on the various process and exposure tools that are used to carry out the subsequent processing steps. The particulates may be transferred, while the wafer is within the process tool or exposure tool, onto a device region on the wafer and create defects which may cause the device to fail. As a result, the process yield of the devices is diminished.

**[0006]** It is therefore desirable to provide a process that reduces the particulate contamination caused by the shining spots.

SUMMARY OF THE INVENTION

**[0007]** The present invention limits the effects of the shining spots that are present at the edge of the wafer by providing a ring of resist or other organic material at the periphery of the wafer to separate the device areas of the wafer from the edge of the wafer where the shining spots are located.

**[0008]** In accordance with an aspect of the invention, devices formed in a substrate are protected from shining spots present in a periphery of the substrate. A ring of material

is formed atop the substrate to separate the periphery of the substrate from a further region of the substrate wherein the devices are formed.

**[0009]** According to another aspect of the invention, at least one device is formed in a substrate. A layer of resist is deposited atop the substrate. The layer of resist is patterned to form a ring of resist atop the substrate. The ring of resist separates a periphery of the substrate from a further region of the substrate, thereby protecting devices formed in the further region of the substrate from shining spots present in the periphery atop the substrate. A further layer of resist is deposited on the substrate. The further layer of resist is patterned to form at least one patterned region within the further region of the substrate.

**[0010]** According to yet another aspect of the invention, a semiconductor device is formed in a substrate in the manner described above.

**[0011]** According to a further aspect of the invention, at least one device is formed in a substrate. A pad oxide layer is deposited atop the substrate, and a pad nitride layer is deposited atop the pad oxide layer. A hard mask layer is deposited atop the pad nitride layer, and a layer of resist is deposited atop the hard mask layer. The layer of resist is patterned to form a ring of resist which separates a periphery of the substrate from a further region of the substrate, thereby protecting devices formed in the further region of the substrate from shining spots present in the periphery of the substrate. A further layer of resist is deposited atop the hard mask layer and atop the ring of resist, and the further layer of resist is patterned to form at least one patterned region within the further region of the substrate. The ring of resist is of sufficient thickness that a region of the further layer of resist that is atop the ring of resist is not patterned. The hard mask layer is etched using the patterned further layer of resist and the ring of resist as an etch mask. At least one trench region in the substrate is etched

using the hard mask layer and the ring of resist as an etch mask. The ring of resist is of sufficient thickness such that a region of the hard mask layer that is beneath the ring of resist remains after the trench region is etched.

**[0012]** The foregoing aspects, features and advantages of the present invention will be further appreciated when considered with reference to the following description of the preferred embodiment and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

**[0013]** Fig. 1 is a diagram showing a known device layout on a substrate in which a device array region directly contacts the shining spot region located at the edge of the wafer.

**[0014]** Figs. 2A-2F are diagrams showing a cross-sectional view of a wafer which is processed in accordance with the invention.

**[0015]** Fig. 3 is a diagram showing a layout of a wafer in which the array area is isolated from the shining spot region at the edge of the wafer in accordance with the invention.

DETAILED DESCRIPTION

**[0016]** Fig. 1 shows a known layout of a portion of a wafer. A vertical DRAM device, or other device, is formed in an array area 102 of the wafer. A plurality of shining spots are formed in an edge region 104 of the wafer. The array region 102 and the edge region 104 are adjacent to one another so that contamination from particulates that break off from the shining spot regions are transferred onto the device features of the array regions 102. The particulates are typically about the same size or of greater size than the feature sizes of the devices in the array region and therefore cause defects and device failures that reduce the process yields.

**[0017]** The present invention therefore provides a ring of resist or other organic materials that separates the array region from the periphery of the wafer and protects the array area from the shining spots of the wafer edge.

**[0018]** Figs. 2A-2F illustrate the steps of a process according to the invention.

**[0019]** Fig. 2A shows a cross-section of a hard mask layer 202 that is formed atop a substrate (not shown), which may be a pad nitrate layer formed over a pad oxide layer and over a silicon substrate as described above. A resist layer 204, such as a photoresist or other resist, is deposited atop the layer 202. Then, as Fig. 2C shows, a portion of the resist is exposed in a known manner, such as by transmitting light through one or more openings in a mask into a projection lens to focus a pattern onto the substrate. When the resist is a negative resist, the periphery region 204a is exposed so that the unexposed region 204b may be subsequently removed when the resist is developed. Alternatively, when the resist is a positive resist, the region 204b is exposed and is removed when the resist is developed so that only the periphery region 204a remains. Fig. 2D illustrates the resist ring 206 that remains after the exposure and development steps.

**[0020]** Then, as Fig. 2E shows, a further layer of resist 208 is deposited atop the exposed regions of the layer 202 as well as atop the resist ring 206. Next, as shown in Fig. 2F, the resist layer 208 is patterned in a known manner to form features 210 in the device regions. The resist ring 206 raises the height of the resist layer 208 above the plane of exposure so that no patterns are formed in the resist layer 208 that is deposited atop the resist ring 206. Moreover, any patterns that may be formed in the portion of the resist layer 208 that is deposited atop the resist ring 206 will not be transferred through the thick resist ring onto the hard mask layer.

**[0021]** Then, the patterned resist features 210 serve to mask the etching of the hard mask layer 202 as does the resist ring 206. The second resist layer 208 may then be removed, but the resist ring 206 remains so that during subsequent deep trench etching, the portion of the hard mask layer at the periphery of the wafer is protected by the resist ring which prevents the removal of the hard mask layer in these regions, thereby preventing the formation of shining spots. Moreover,

any shining spots that are formed at the edge of the wafer are isolated from the device regions.

**[0022]** FIG. 3 shows a top view of a layout of a wafer. A device region 302 is isolated from the edge of the wafer 304, where shining spots are formed, by a separation region 306 which is formed beneath the resist ring 206, shown in FIG. 2. The separation between the shining spots and the device region protects against the transfer of particulates generated in the shining spot regions onto the device region, and reduces the generation of defects. As a result, device yields is increased.

**[0023]** Alternatively, a ring of resist, or other organic material, is deposited directly onto the periphery of the wafer to form the ring 206 shown in FIG. 2D without a lithographic step. Then, the further resist layer 208 may be deposited and patterned as shown in FIGS. 2E and 2F.

**[0024]** Advantageously, the invention avoids the formation of shining spots near the edge of the wafer and protects from the effects of any shining spots that are formed at the edge of the wafer. As a result, fewer defects are formed in the device regions of the wafer, so that the device yields increases and reduces the production costs of the devices.

**[0025]** Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended claims.